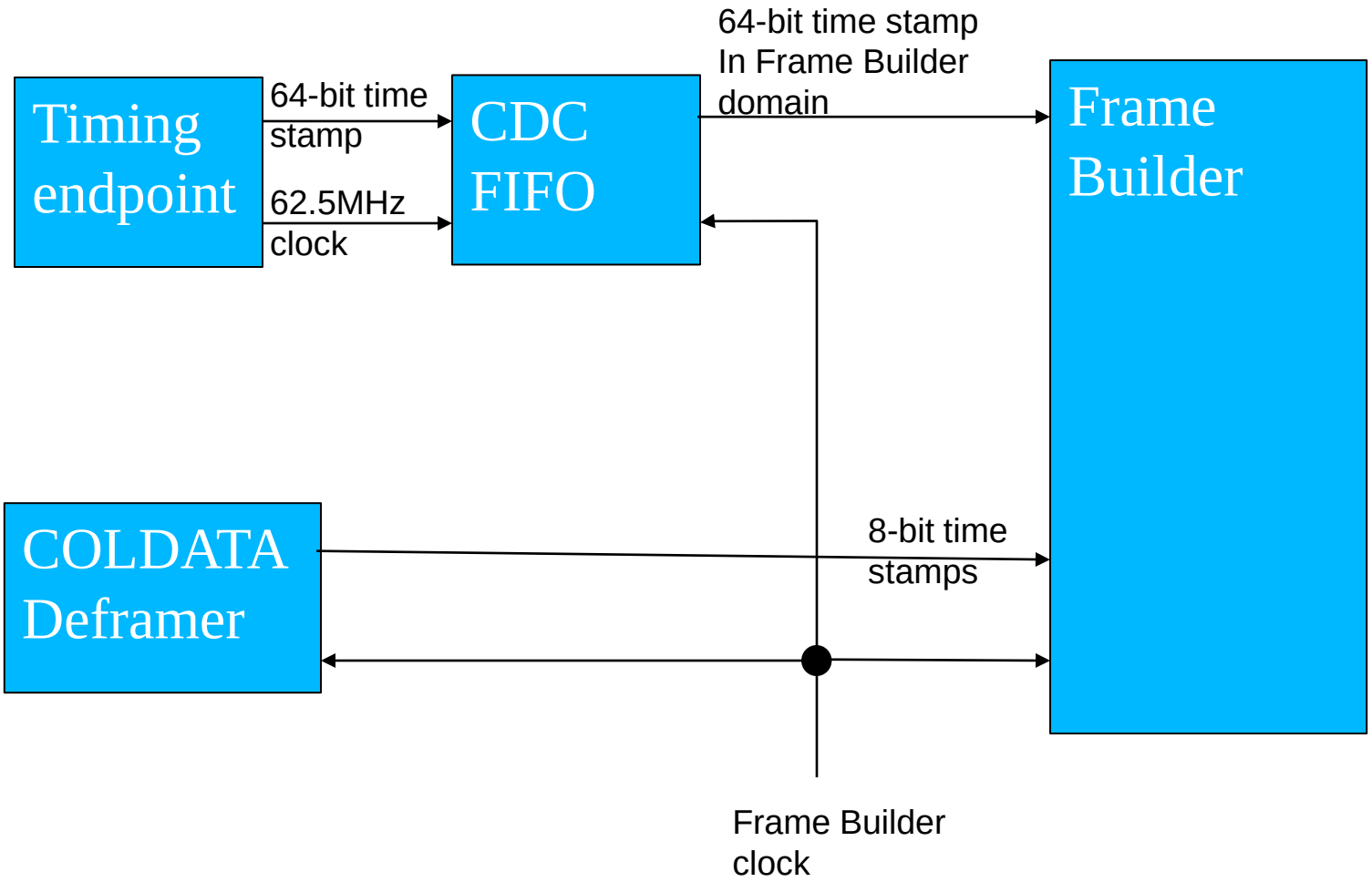
Time stamp jitter

- **Current firmware version at ICEBERG:**
  - **Does not have TLU (64-bit) time stamp clock domain crossing logic**
  - **That means that depending on Frame Builder clock phase, the time stamp may be recorded unreliably**
  - **Manifests as jitter in lower bits**
  - **Occasional large jumps are possible, when many bits at once are changing at the “bad” time relative to Frame builder clock**
- **Another reason for time stamp jitter:**
  - **COLDATA serial links are asynchronous to system clock (62.5MHz)**
  - **COLDATA frames arrive with time jitter of 1 clk relative to 62.5M clock**
  - **This cannot be fixed**

Time stamp reclocking

- **Working on adding the proper Clock Domain Crossing now, a.k.a. CDC, a.k.a. reclocking**



Time stamps

Frame Builder logic for time stamps:

- 64-bit time stamp is locked for transmission when frames from all links arrived
- 8-bit time stamps come with data from each link, they are transmitted with the data from their native COLDATA frame

TLU trigger

- Work ongoing
- According to plan from last meeting
- Should be ready tomorrow